Narasinga Rao Miniskar, Ph.D.

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Summary:
Strong research and exploration skills combined with technical expertise helps me to understand the challenges in HPC and embedded systems and adapt to the environment to make significant contributions in these domains.

Appointments:

- **Research Software Engineer (ORNL) from July 2019.** Research work includes heterogenous systems, RISC-V architecture exploration, hardware scheduling algorithms, and applying Machine Learning approaches for system architecture problems such as design space exploration, scheduling, IRIS run-time framework.
- **Principal Engineer/Associate Architect at Samsung R&D India Bangalore (SRIB) from Nov-2011 to July 2019.** Responsibilities include project management, research proposals, leading the team with solutions and research direction, mentoring graduate and post graduate interns from prestigious institutions in India. Research work on compiler for deep learning architectures, inference framework and models to enable AI for mobile devices, and also DNN accelerator platform cycle accurate simulators. Past experience on reconfigurable processor (CGRA) architectures and development tool chain such as compiler, cycle accurate simulators, and profilers. Developed an industry best high performance, low memory and light weight DNN fixed point framework for ARM Big.Little architectures.
- **Research Scholar at IMEC R&D, Belgium from Oct-2006 to Oct-2011.** Proposed a system scenario based methodology for energy efficient multiprocessor resource management for embedded systems.
- **Senior Software Engineer at Agere Systems India Pvt. Ltd, Bangalore from July-2002 to Oct-2006.** Worked on the development of customizable software traffic generator for wide range of Agere network processors.

EDUCATION:

- **Doctor in Engineering (Ph.D.) from IMEC & K.U.Leuven on Dec-2012** (Oct 2006 – Oct 2011)
- **Master of Technology (M.Tech)** in **Computer Science & Engineering**
  Indian Institute of Technology Delhi, India. (July 2002 – May 2004)
- **Bachelor of Technology (B.Tech.)** in **Computer Science & Engineering**
  J.N.T.University, Hyderabad, A.P., India. (Sep 1998 – May 2002)
- **Diploma in Computer Science & Engineering**
  Govt S.V.Polytechnic College, Tirupati, A.P., India. (Sep 1995 – May 1998)

PATENTS:

- [Patent] Method and apparatus for determining memory requirement in a network, US20200257972A1, US11593644B2
- [Patent] Memory Efficient Lock-Free Circular Queue - Split Indexing with Odd-Even Increment, US20220129275A1
- [Patent]: A Hardware-Assisted Task Scheduling for Extremely Heterogeneous Accelerators, US20220188155A1

PUBLICATIONS:

- Article: A 3D Implementation of Convolutional Neural Network for Fast Inference. Narasinga Rao Miniskar, Pruek Vanna-iampikul, Aaron Young, Sung Kyu Lim, Frank Liu, Jieun Yoo, Corrinne Mills, Nhan Tran, Farah Fahim, Jeffrey S Vetter. IEEE International Symposium on Circuits and Systems (ISCAS) 2023 May.

- Article: Tiling Framework for Heterogeneous Computing of Matrix-Based Tiled Algorithms. Narasinga Rao Miniskar, Mohammad Alaul Haque Monil, Pedro Valero-Lara, Frank Liu, Jeffrey S. Vetter. In Proceedings of The 2nd International Workshop on Extreme Heterogeneity Solutions (PPOPP ExHET Workshop'23). 2023.

- Article: A survey on processing-in-memory techniques: Advances and challenges. Asifuzzaman, Kazi, Narasinga Rao Miniskar, Aaron R. Young, Frank Liu, and Jeffrey S. Vetter. Journal Memories-Materials, Devices, Circuits and Systems (2023), Elsevier publisher, Volume 4.

- Article: IRIS-BLAS: Towards a Performance Portable and Heterogeneous BLAS Library, Narasinga Rao Miniskar, Mohammad Alaul Haque, Pedro Valero-Lara, Frank Y. Liu, Jeffrey S. Vetter. 29th IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC) 2022.

- Article: LaRIS: Targeting Portability and Productivity for LAPACK Codes on Extreme Heterogeneous Systems by Using IRIS. Monil, Mohammad Alaul Haque, Narasinga Rao Miniskar, Frank Y. Liu, Jeffrey S. Vetter, and Pedro Valero-Lara. In 2022 IEEE/ACM Redefining Scalability for Diversely Heterogeneous Architectures Workshop (RSDHA), pp. 12-21. IEEE, 2022.

- Article: Ultra low latency machine learning for scientific edge applications. Miniskar, Narasinga Rao, Aaron Young, Frank Liu, Willem Blokland, Anthony Cabrera, and Jeffrey Vetter. 32nd International Conference on Field Programmable Logic and Applications hosted by Queens University Belfast, United Kingdom, 2022.

- Article: Adrastea: An Efficient FPGA Design Environment for Heterogeneous Scientific Computing and Machine Learning. Young, A.R., Miniskar, N.R., Liu, F., Blokland, W., Vetter, J.S. (2022). In: Doug, K., Al, G., Pophale, S., Liu, H., Parete-Koon, S. (eds) Accelerating Science and Engineering Discoveries Through Integrated Research Infrastructure for Experiment, Big Data, Modeling and Simulation. SMC 2022. Communications in Computer and Information Science, vol 1690. Springer, Cham.

- Article: Toward Performance Portable Programming for Heterogeneous Systems on a Chip: A Case Study with Qualcomm Snapdragon SoC. Cabrera, Anthony, Seth Hitefield, Jungwon Kim, Seyong Lee, Narasinga Rao Miniskar, and Jeffrey S. Vetter. In 2021 IEEE High Performance Extreme Computing Conference (HPEC), pp. 1-7. IEEE, 2021.

- Article: A Hierarchical Task Scheduler forHeterogeneous Computing, Narasinga Rao Miniskar, Frank Liu, Aaron Young, Dwaipayan Chakraborty, Jeffey Vetter, ISC-HPC 2021

- Article: Memory efficient lock-free circular queue, Narasinga Rao Miniskar, Frank Liu, Jeffrey S. Vetter. IEEE International Symposium on Circuits and Systems (ISCAS) 2021 May, 26

- Article: Deffe: a data-efficient framework for performance characterization in domain-specific computing. Frank Liu, Narasinga Rao Miniskar, Dwaipayan Chakraborty, and Jeffrey S. Vetter. 2020. In Proceedings of the 17th ACM International Conference on Computing Frontiers (CF '20). Association for Computing Machinery, New York, NY, USA, 182–191.

- Article: Light Weight and Fast Simulation Methodology in SystemC for TLM based Behavior Modeling of Programmable Processors. Shashidhar SK, Miniskar NR, Batchu SK, Kim K. In 2019 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT) 2019 Jul 26 (pp. 1-7). IEEE.

- Article: Low Complex & High Accuracy Computation Approximations to Enable On-Device RNN Applications. Pasupuleti SK, Gadde RN, Rajagopal V, Vishnoi A, Sekhar NC, Kumar RC, Miniskar NR. In 2019 IEEE International Symposium on Circuits and Systems (ISCAS) 2019 May 26 (pp. 1-5).

- Article: Optimal SDRAM buffer allocator for efficient reuse of layer IO in CNNs inference framework. Miniskar NR, Pasupuleti SK, Rajagopal V, Vishnoi A, Ramasamy CK, Gadde RN. In 2018 IEEE International Symposium on Circuits and Systems (ISCAS) 2018 May 27

- Article: An Intelligent Bandwidth Manager for CNN Applications on Embedded Devices. Pasupuleti SK, Rajaram A, Miniskar NR, Gadde RN, Yadvandu D, Rajagopal V, Vishnoi A, Ramasamy CK. In 2018 25th IEEE International Conference on Image Processing (ICIP) 2018 Oct 7 (pp. 4173-4177).

- Article: Accurate and efficient fixed point inference for deep neural networks. Rajagopal V, Ramasamy CK, Vishnoi A, Gadde RN, Miniskar NR, Pasupuleti SK. In 2018 25th IEEE International Conference on Image Processing (ICIP) 2018 Oct 7 (pp. 1847-1851). IEEE.

- Article: Fast cycle-accurate compile based simulator for reconfigurable processor. Miniskar NR, Gadde RN, Cho YC, Kim S. In 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 2017 May 28 (pp. 1-4). IEEE.

- Article: A novel method to regenerate an optimal CNN by exploiting redundancy patterns in the network. Pasupuleti SK, Miniskar NR, Rajagopal V, Gadde RN. In 2017 IEEE International Conference on Image Processing (ICIP) 2017 Sep 17 (pp. 4407-4411).

- Article: Intra mode power saving methodology for cgra-based reconfigurable processor architectures. Miniskar NR, Patil RR, Gadde RN, Cho YC, Kim S, Lee SH. In 2016 IEEE International Symposium on Circuits and Systems (ISCAS) 2016 May 22 (pp. 714-717).

- Article: Retargetable automatic generation of compound instructions for CGRA based reconfigurable processor applications. Miniskar NR, Kohli S, Park H, Yoo D. In Proceedings of the 2014 International Conference on Compilers, Architecture and Synthesis for Embedded Systems 2014 Oct 12 (p. 4). ACM. (pp. 1-9).

- Article: Function inlining and loop unrolling for loop acceleration in reconfigurable processors. Miniskar NR, Gode PS, Kohli S, Yoo D. In Proceedings of the 2012 international conference on Compilers, architectures and synthesis for embedded systems 2012 Oct 7. ACM.

- Article: Memory and communication driven spatio-temporal scheduling on MPSoCs. Bhatti ZW, Miniskar NR, Preuveneers D, Wuyts R, Berbers Y, Catthoor F. In 2012 25th Symposium on Integrated Circuits and Systems Design (SBCCI) 2012 (pp. 1-6). IEEE.

- Article: SAMOSA: Scratchpad aware mapping of streaming applications. Bhatti ZW, Preuveneers D, Berbers Y, Miniskar NR, Wuyts R. In 2011 International Symposium on System on Chip (SoC) 2011 (pp. 48-55). IEEE.

- Article: PinComm: Characterizing intra-application communication for the many-core era. Heirman W, Stroobandt D, Miniskar NR, Wuyts R, Catthoor F. In 2010 IEEE 16th International Conference on Parallel and Distributed Systems 2010 Dec 8 (pp. 500-507).

- Article: Scenario based mapping of dynamic applications on mpsoc: A 3d graphics case study. Miniskar NR, Hammari E, Munaga S, Mamagkakis S, Kjeldsberg PG, Catthoor F. In International Workshop on Embedded Computer Systems 2009 Jul 20 (pp. 48-57). Springer.

WORKSHOP and TECH REPORTS:
- TECH REPORT: ORNL COSMIC: APRIL 2021 REPORT: Performance portable toolchain for Streaming applications (5G Software Defined Radio) on Heterogeneous Architectures
- ASCR Workshop: Heterogeneous Memory System Framework for HPC, Kazi Asifuzzaman, Narasinga Rao Miniskar, Aaron R. Young, Frank Liu, Jeffrey S. Vetter, ASCR Workshop on the Management and Storage of Scientific Data Jan, 2022.
- ASCR Workshop: Emerging Heterogeneous Systems Provide Great Opportunities for Codesign, Aaron R. Young, Jeffrey S. Vetter, Frank Liu, Narasinga Rao Miniskar, Sarat Sreepathi, and Anthony M. Cabrera, ASCR Workshop on Reimagining Codesign, Mar 2021

TEACHING ASSISTANT:
- Teaching assistant for advanced architectures and exploration course work during Ph.D. for master students in K.U.Leuven for the duration from 2007 to 2011

HONORS:
- Two times winner of worldwide Samsung Best Paper Bronze award in (SBPA-2013, 2017)
- All India 72nd rank in CS stream of Graduate Aptitude Test of Engineering (GATE-2002), an entrance test for engineering post-graduation in Indian universities
- Second prize in IEEE-2002 annual technical symposium and software contest, IIT-Roorkee